SUMMiT V™
Five Level Surface Micromachining Technology
Design Manual

Version 3.2 – October 25, 2012

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SAND 2010-6786 P

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Overview and Technology Description

SUMMiT V™ (Sandia Ultra-planar Multi-level MEMS Technology V) is a 1.0 micron, 5-level, surface micromachining (SMM) technology featuring four mechanical layers of polysilicon fabricated above a thin highly doped polysilicon electrical interconnect and ground plane layer. Sacrificial oxide is sandwiched between each polysilicon level. The thin sacrificial film defines the amount of mechanical play in gear hubs and hinges. The oxide directly beneath the upper two levels of mechanical polysilicon are planarized using a chemical mechanical polishing (CMP) process, which alleviates several photolithographic and film etch issues while freeing the designer from constraints that would otherwise be imposed by the underlying topography. An optional patterned metal layer can be applied to the top polysilicon layer for electrical connections.

The entire stack, shown below in Figure 1, is fabricated on a 6-inch single crystal silicon wafer with a dielectric foundation of 0.63µm of oxide and 0.80µm of nitride.

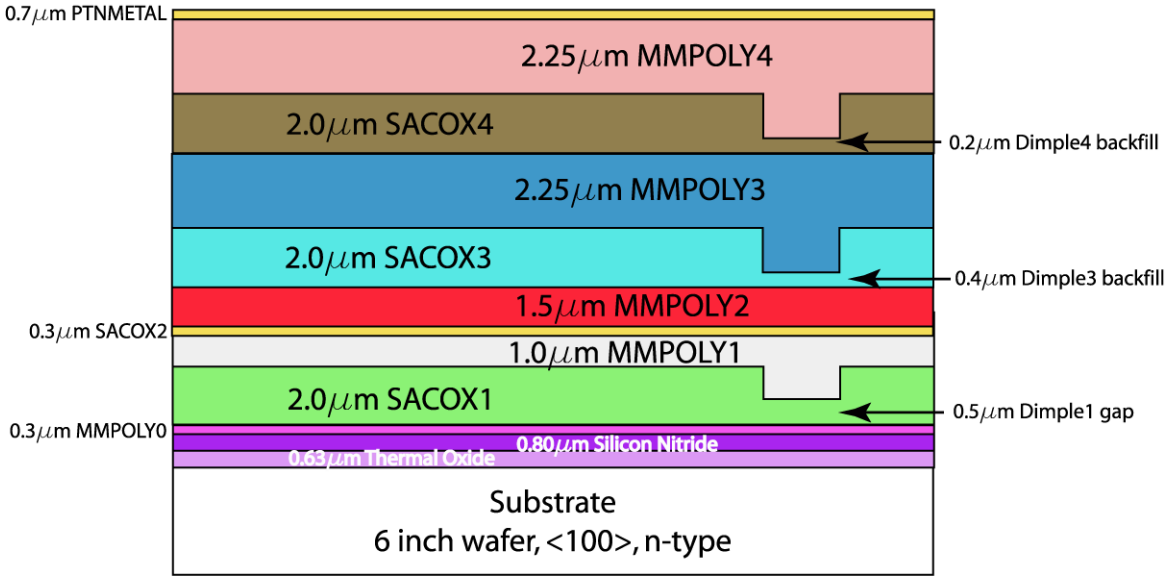


Figure 1: Drawing of the SUMMiT V™ structural and sacrificial layers

The layers of polysilicon are designated from the substrate up as MMPOLY0 through MMPOLY4. Prefixing these levels with “MM” for micromechanical prevents confusion with layer names often used in CMOS processes. The sacrificial films are designated as SACOX1 through SACOX4, with the numerical suffix corresponding to the number of the subsequent layer of mechanical polysilicon that is deposited on a given oxide. The patterned (PTN) metal layer is designated PTNMETAL.

The cross section in Figure 2 represents the various types of features that can be created from the 14 individual masks defined in Table 1 and the SUMMiT V™ fabrication sequence.

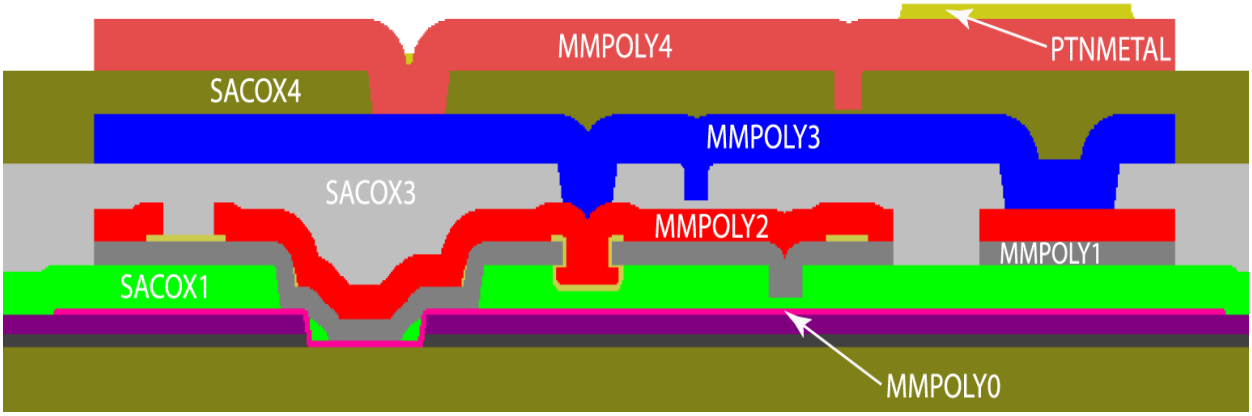


Figure 2: Cross-section of SUMMiT V stack showing features realizable through the fabrication process.

SUMMiT V™ MASKING LAYERS

Table 1 : SUMMiT V™ MASKING LAYERS

MASK NAME	MASK LEVEL	FIELD	ALIGNS TO LEVEL*	PRIMARY PURPOSE	LAYER NUMBER (GDSII)
NITRIDE_CUT (NIC)	1	**DARK**	**N/A**	Substrate contacts	21
MMPOLY0 (P0)	2	**CLEAR**	**NITRIDE_CUT**	Ground plane and electrical interconnects	22
DIMPLE1_CUT (D1C)	3	**DARK**	**MMPOLY0**	Dimples in MMPOLY1	23
SACOX1_CUT (X1C)	4	**DARK**	**MMPOLY0**	Anchor for MMPOLY1	24
PIN_JOINT_CUT (PJC)	5	**DARK**	**MMPOLY0**	Cut in MMPOLY1 with constraint flange	26
MMPOLY1_CUT (P1C)	6	**DARK**	**MMPOLY0**	Cut in MMPOLY1 without constraint flange	25
SACOX2 (X2)	7	**CLEAR**	**MMPOLY0**	Defines hub/hinge play	27
MMPOLY2 (P2)	8	**CLEAR**	**MMPOLY0**	Patterns MMPOLY2 and/or MMPOLY1 + MMPOLY2	28
DIMPLE3_CUT (D3C)	9	**DARK**	**MMPOLY0**	DIMPLEs in MMPOLY3	29
SACOX3_CUT (X3C)	10	**DARK**	**MMPOLY0**	Anchor MMPOLY3	30
MMPOLY3 (P3)	11	**CLEAR**	**SACOX3_CUT**	Patterns MMPOLY3	31
DIMPLE4_CUT (D4C)	12	**DARK**	**MMPOLY0**	DIMPLEs in MMPOLY4	34
SACOX4_CUT (X4C)	13	**DARK**	**MMPOLY0**	Anchor MMPOLY4	42
MMPOLY4 (P4)	14	**CLEAR**	**SACOX4_CUT**	Patterns MMPOLY4	36
PTNMETAL (PTN)	15	**CLEAR**	**MMPOLY4**	Patterns PTNMETAL	48

* Alignment tolerance to reference layer is better than 0.5μm.

Drawing Only Layers

In addition to the layers shown in Table 1, five have been created to facilitate layout and are referred to as "drawing only" layers. Listed in Table 2, these layers do not directly define a mask, but are instead XORed with their corresponding master layer to define the mask used during the fabrication process.

Table 2: SUMMiT V™ DRAWING ONLY LAYERS

LAYER NAME	XORed WITH LAYER	PRIMARY PURPOSE	LAYER NUMBER (GDSII)
MMPOLY0_CUT (P0C)	P0	Define holes/openings within a MMPOLY0 boundary	62
MMPOLY1 (P1)	P1C	Define MMPOLY1 within a MMPOLY1_CUT boundary	35
SACOX2_CUT (X2C)	X2	Define holes/openings within a SACOX2 boundary	37
MMPOLY2_CUT (P2C)	P2	Define holes/openings within a MMPOLY2 boundary	38
MMPOLY3_CUT (P3C)	P3	Define holes/openings within a MMPOLY3 boundary	41
MMPOLY4_CUT (P4C)	P4	Define holes/openings within a MMPOLY4 boundary	46
PTNMETAL_CUT (PTNC)	PTNMETAL	Define holes/openings within a PTNMETAL boundary	59

Layer Naming

Simply associating a drawing layer with either a clear field or dark field mask can sometimes lead to ambiguous interpretations about what gets etched and what remains on the wafer. This is further complicated when multiple drawing layers are combined at the mask house to generate the actual mask. The following naming convention is being used to eliminate this confusion:

If: the drawing layer name ends with the suffix "**_CUT**"
Then: geometry drawn on this layer defines what gets etched away
Otherwise: Geometry defines what remains after etching

Anchor Cuts

Anchor cuts are normally intended to anchor one layer of polysilicon to the polysilicon layer immediately below it in the fabrication sequence:

X(n)C anchors P(n) to P(n-1) n=1,2,3,4

Except for P0, the SUMMiT V™ design rules do not require full enclosure of the P(n-1) layer about the X(n)C geometry. If, however, the overlap of X(n)C and P(n-1) is insufficient to form a reliable anchor or there is no overlap at all between these two layers, the condition is flagged as an "invalid sacoxn anchor".

DIMPLE Cuts

Dimple cuts are similar to anchor cuts, but they do not physically anchor to the underlying P(n-1) layers described in the previous section. The DIMPLE1_CUT is formed by a timed etch designed to stop after penetrating 1.5μm into the 2μm thick SACOX1, leaving a 0.5μm clearance beneath the dimple. A timed etch is possible because the SACOX1 thickness can be well controlled. CMP processing of the SACOX3 and SACOX4 leads to thickness variations that makes pure timed approaches to creating dimple cuts less viable in these layers. Therefore, the DIMPLE3_CUT is designed to etch all the way down to MMPOLY2 much like the anchor cut is formed. Then 0.4μm of oxide is deposited as backfill to control the dimple clearance. DIMPLE4_CUT is similarly performed, with the backfill being just 0.2μm.

PIN JOINT Cuts

Pin joint cuts are formed by first patterning MMPOLY1 with the PIN_JOINT_CUT mask. This same geometry (typically a circle) is etched into SACOX1 and undercut the MMPOLY1 to form the flange. The resulting cavity is lined with SACOX2 and backfilled with MMPOLY2.

MMPOLY1 and SACOX2 Mask Polarity

The mask that patterns MMPOLY1 is a dark field mask, whereas the other MMPOLY layers are light field. Consistent with the previously stated naming convention, the mask name associated with MMPOLY1 patterning is "MMPOLY1_CUT" and not MMPOLY1. Likewise, the SACOX2 mask has the opposite mask polarity from the other sacox masks. By default, MMPOLY1 remains after the MMPOLY1 etch, and SACOX2 is removed during the SACOX2 etch. Reversal of the mask polarity can be simulated by defining a boundary of MMPOLY1_CUT and by drawing a region of SACOX2 within this boundary. A MMPOLY1 structure can then be drawn as normal within a MMPOLY1_CUT region, and SACOX2_CUT can be defined within a region of SACOX2. Note that this process is not recursive. A MMPOLY1_CUT within a MMPOLY1 boundary that is itself contained with a MMPOLY1_CUT is not illegal, but it will not produce the desired result.

MMPOLY1 Definition

A total of 7 drawing layers together with the fabrication sequence define the actual geometry of MMPOLY1 defined here as P1''. The Boolean expression for the contribution of these layers follows:

P1C = PIN_JOINT_CUT .AND. MMPOLY1_CUT
P1' = NOT (P1C .XOR. MMPOLY1)
P2' = MMPOLY2 .XOR. MMPOLY2_CUT
X2' = SACOX2 .XOR. SACOX2_CUT
X2'' = P2' .OR. X2'
P1'' = P1' .AND. X2''

In less precise terms P1 is defined in the following way in the layout tool. Without any other layers, a polygon drawn in MMPOLY1 will not be fabricated. In the same way, a polygon drawn in SACOX2_CUT without the aid of other layers will not survive the fabrication process. A polygon drawn in MMPOLY1_CUT will be fabricated as will the intersection of MMPOLY1 and SACOX2 polygons inside it. If a SACOX2 polygon is drawn without a MMPOLY1_CUT covering it, the result is a MMPOLY1 structure.

Annotation Layers

In addition to the layers shown in Table 1 and 2, layers have been defined to facilitate drawing annotation and are referred to as annotation layers. These layers are not used to define any mask and are not checked by the DRC.

LAYER NAME	PRIMARY PURPOSE
0	Used for block placement.
CONSTRUCTION	Used for temporary construction lines.
DIMEMSION	Used for dimensions.
NOTES	Used for text notes and other documentation.
TEMP	Used for drawing temporary geometry.

Electrical Properties

All polysilicon layers are n-type. The substrate is a 6-inch n-type <100> silicon wafer with resistivity of 2-20 Ω cm.

Table 3 shows the sheet resistance of each of the layers expressed in Ω/square. These tests are performed using Van der Pauw structures at multiple locations across a quarter wafer (see Ref 1). Table 4 shows the contact resistance for vias between different layers, where the via is drawn as a 4x4µm square. The contact resistance test structures are similar to Van der Pauw structures.

Table 3: SHEET RESISTANCE (ohm/sqr.)

Layer	Mean	Std. Dev. of mean	Pooled StDev	Avg Sample StDev
MMPOLY0	33.99	5.14	5.35	1.141
MMPOLY1	23.66	1.70	1.85	0.345
MMPOLY2	21.94	0.82	0.85	0.202
MMPOLY1_2	9.64	0.34	0.36	0.086
MMPOLY3	8.43	0.26	0.28	0.091
MMPOLY4	9.01	0.23	0.27	0.098
PTNMETAL	0.042	---	---	---

Table 4: CONTACT RESISTANCE (ohms) for 4x4µm vias

Layer	Mean	Std. Dev. of mean	Pooled StDev	Avg Sample StDev
P0 to P1	15.16	0.79	0.84	0.283
P0 to P1_2	14.46	0.54	0.60	0.268
P1_2 to P3	10.14	0.58	0.65	0.295
P1 to P2	11.32	0.38	0.39	0.101
P2 to P3	11.90	0.54	0.61	0.273
P3 to P4	9.26	0.43	0.50	0.243

Mean: The overall arithmetic mean of the resistance measurements (x-bar)
StDev of Mean: The standard deviation of x-bar
Pooled StDev: The pooled standard deviation
Avg Sample StDev: This is the average sample standard deviation, where each sample consists of about 7-12 measurements from a quarter wafer. Each measurement is actually the average of 4 resistance values.

Layer Thickness

Table 5: LAYER THICKNESS

Layer	Mean (µm)	Std. Dev. (Å)
MMPOLY0	.29	20
SACOX1	2.04	210
DIMPLE1 Depth	-	-
MMPOLY1	1.02	23
SACOX2	.3	44
MMPOLY2	1.53	34
SACOX3	1.84	5400
DIMPLE3 Backfill	.4	53
MMPOLY3	2.36	99
SACOX4	1.75	4500
DIMPLE4 Backfill	.21	30
MMPOLY4	2.29	63

Beam Width Measurements

The width of polysilicon beams are measured routinely using a calibrated SEM to monitor edge bias. Table 6 gives the as-drawn dimension of the beams and the resulting beam widths. Usually, 10 measurements are taken per lot, at 5 locations on 2 different wafers. The beams are normally narrower than the as-drawn dimension due to edge bias that results from the lithography and etching processes.

Designers should take this into account when creating designs that rely on specific beam widths. See the Sandia MEMS Short Course Materials and Refs 1-2 for more information about edge bias.

Table 6: BEAM WIDTH DATA (µm)

Layer	As-Drawn	Mean	Std. Dev. of mean	Pooled StDev	Avg Sample StDev
MMPOLY2	1.000	0.872	0.059	0.066	0.027
MMPOLY3	1.000	0.775	0.061	0.065	0.024
MMPOLY4	2.000	1.665	0.077	0.082	0.030

As-Drawn: The dimension of the linewidth feature as drawn in AutoCAD
Mean: The overall arithmetic mean of the linewidth measurements (x-bar)
StDev of Mean: The standard deviation of x-bar
Pooled StDev: The pooled standard deviation
Avg Sample StDev: The average sample standard deviation, where each sample consists of about 5 measurements taken on 2 wafers from a single lot

[1] Limary, S., Stewart, H.D., Irwin, L.W., McBrayer, J., Sniegowski, J.J., Montague, S., Smith, J.H., de Boer, M.P., and Jakubczak, J.F., 1999, "Reproducibility data on SUMMiT," Proceedings of SPIE - The International Society for Optical Engineering, Vol. 3874, pp. 102-112.
[2] Tanner, D.M., Owen, A.C., Jr., and Rodriguez, F., 2003, "Resonant Frequency Method for Monitoring MEMS Fabrication," Proceedings of SPIE - The International Society for Optical Engineering, Vol. 4980, pp. 220-228.

Design Rules for Individual Layers

1) NITRIDE_CUT

A) MIN WIDTH 1.00
B) MIN SPACE 1.00

Required Layers:

- Edges must be covered by MMPOLY0 & MMPOLY1

C) In most cases SACOX1_CUT should completely cover the NITRIDE_CUT with an overlap of 0.5µm. If SACOX_1 does not cover NITRIDE_CUT completely then it must form a ring around the outside edge of the NITRIDE_CUT. SACOX1_CUT must overlap the outside edge of the nitride cut by at least 0.5µm and by at least 6.5µm on the inside of the nitride cut.

Incompatible Layers:

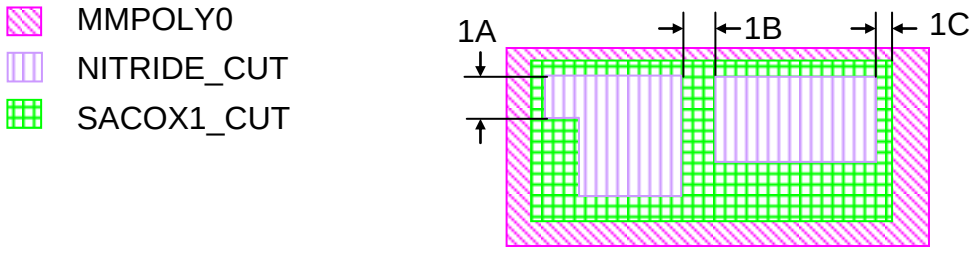
- MMPOLY1_CUT about edges

Notes:

- NITRIDE_CUT cuts down to the substrate removing both the nitride and oxide dielectric layers.
- SACOX3_CUT may not be deep enough to anchor to MMPOLY2 in areas where it overlaps NITRIDE_CUT.
- The pictures below are a graphic representation of the design rules

Errors:

- ERR_NIC_W_LT_1
- ERR_NIC_S_LT_1
- ERR_NIC_EDGE_WO_P0
- ERR_NIC_EDGE_WO_P1



2) MMPOLY0

A) MIN WIDTH 1.00
B) MIN SPACE 1.00

Required Layers:

- None

Incompatible Layers:

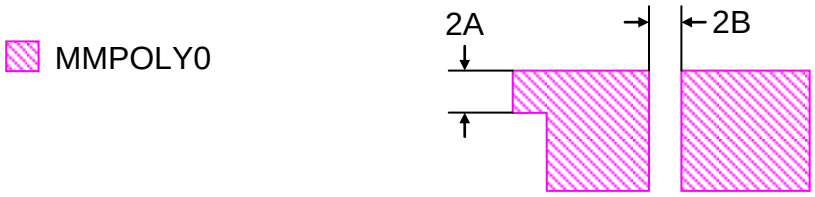
- None

Notes:

- A MMPOLY0 ground plane is recommended beneath structures whenever possible.

Errors:

- ERR_P0_W_LT_1
- ERR_P0_S_LT_1



3) MMPOLY0_CUT

A) MIN WIDTH 1.00

B) MIN SPACE 1.00

Required Layers:

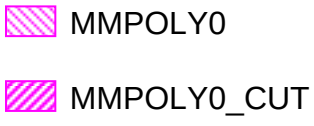
C) MMPOLY0 enclosure of MMPOLY0_CUT = 1.00

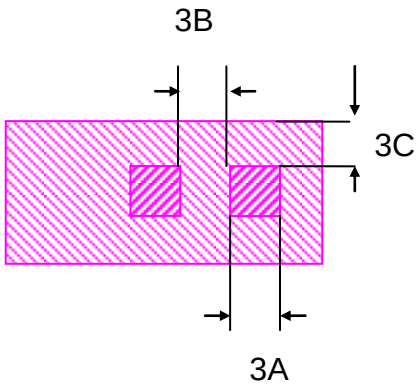
Incompatible Layers:

- None

Errors:

- ERR_P0C_WITHOUT_P0





4) DIMPLE1_CUT

A) MIN WIDTH 1.00
B) MIN SPACE 1.00

Required Layers:

C) MMPOLY1 enclosure of DIMPLE1_CUT= 0.5

Incompatible Layers:

D) SACOX1_CUT space = 1.0
E) PIN_JOINT_CUT space = 1.0
F) MMPOLY1_CUT space = 0.5

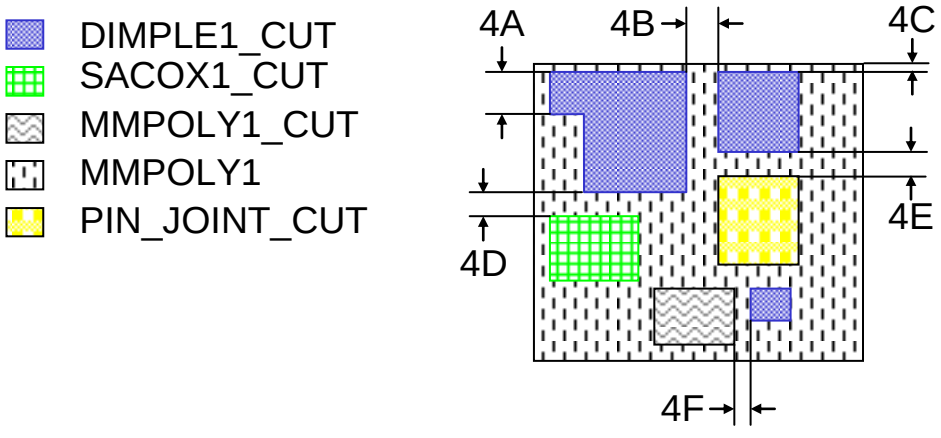
Recommended Layers:

- MMPOLY0

Notes:

Errors:

- ERR_D1C_W_LT_1
- ERR_D1C_S_LT_1
- ERR_D1C_PJC_S_LT_1
- ERR_D1C_P1C_S_LT_0PT5
- ERR_D1C_X1C_S_LT_1
- ADV_D1C_S_GT_75
- ADV_D1C_WITHOUT_P0



5) SACOX1_CUT

A) MIN WIDTH 1.0
with minimum area* = 3.14 μm^2

B) MIN SPACE 1.0

Required Layers:

C) MMPOLY0 enclosure of SACOX1_CUT = 0.5

D) MMPOLY1 enclosure of SACOX1_CUT = 0.5

Incompatible Layers:

E) DIMPLE1_CUT space = 1.0

F) PIN_JOINT_CUT space = 1.0

G) MMPOLY1_CUT space = 0.5

Recommended Layers:

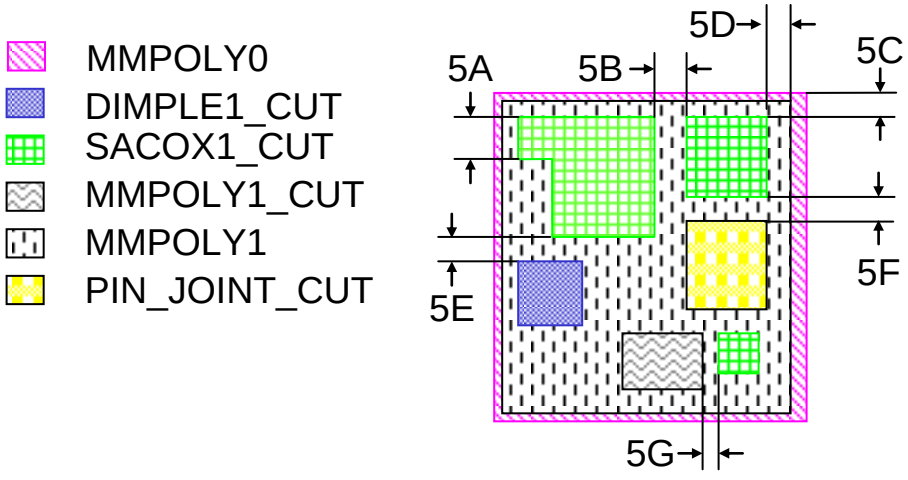
- MMPOLY2 enclosure of SACOX1_CUT = 0.5

Notes:

*Area is based on 2-μm diameter circle, meaning that a circle this size shall fit it at least one location within the SACOX1_CUT boundary. If this is not the case, the rule is flagged as "invalid SACOX1 anchor".

Errors:

- ERR_X1C_W_LT_1
- ERR_X1C_S_LT_1
- ERR_X1C_PJC_S_LT_1
- ERR_X1C_P1C_S_0PT5



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6) PIN_JOINT_CUT

A) MIN WIDTH 3.0
B) MIN SPACE 7.0

Required Layers:

C) MMPOLY1 enclosure of PIN_JOINT_CUT = 1.0
D) SACOX2 enclosure of PIN_JOINT_CUT = 0.5
E) MMPOLY2 enclosure of PIN_JOINT_CUT = 1.0

Incompatible Layers:

F) DIMPLE1_CUT space = 1.0
G) SACOX1_CUT space = 1.0
H) MMPOLY1_CUT space = 1.0
I) SACOX2_CUT space = 0.5
J) MMPOLY2_CUT space =1.0

Recommended Layers:

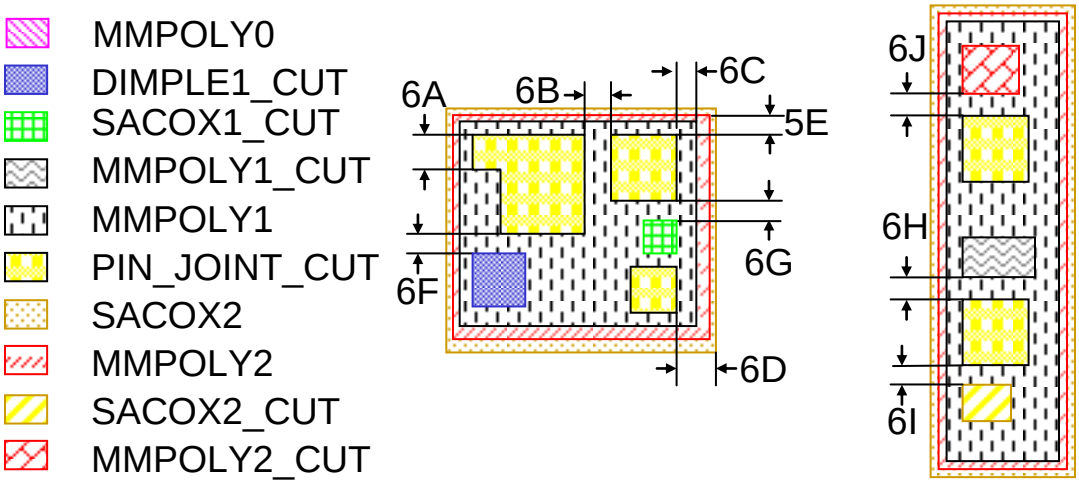
- MMPOLY0: full coverage under path of pin joint

Notes:

To operate as normally intended, adjacent PIN_JOINT_CUTs should be at least 7.0µm apart.
Donut shaped cuts could produce free floaters.

Errors:

- ERR_PJC_W_LT_3
- ERR_PJC_S_LT_1
- ADV_PJC_WITHOUT_P0
- ADV_PJC_S_LT_4



7) SPECIAL RULE ABOUT MMPOLY1 ISLANDS FORMED BY PIN_JOINT_CUT

(*This rule is not yet implemented in the design rules)**

- MIN WIDTH 1.0
  with minimum area* = 3.14 μm^2

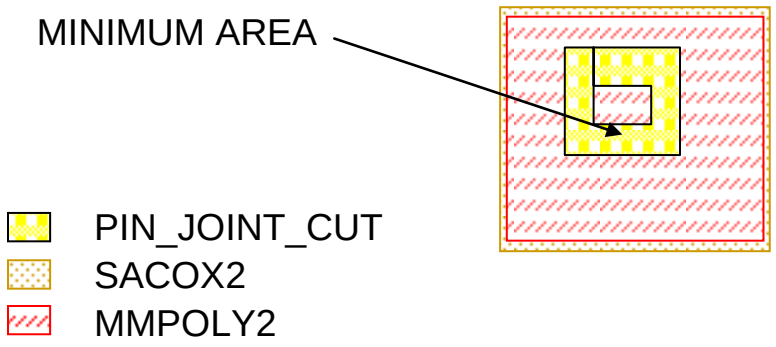
Required Layers:

Incompatible Layers:

Recommended Layers:

Notes:

- Area is based on 2-µm diameter circle, meaning that a circle this size shall fit it at least one location within the MMPOLY1 island formed by the PIN_JOINT_CUT enclosure. If this is not the case, the rule is flagged as "PIN_JOINT_CUT floater".



8) MMPOLY1

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

- MMPOLY1_CUT

Incompatible Layers:

Recommended Layers:

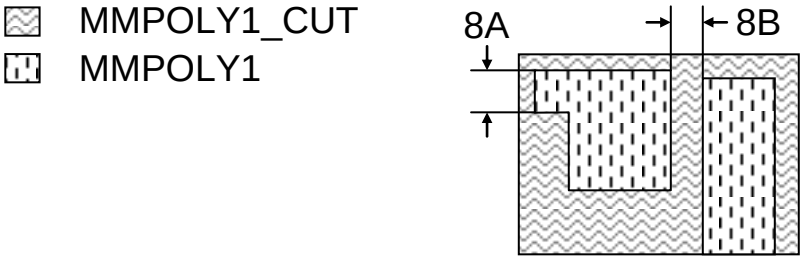
- MMPOLY0 under MMPOLY1

Notes:

- To prevent problems due to electrostatic attenuation between polysilicon structures and the silicon nitride, MMPOLY0 is recommended under all released polysilicon structures.

Errors:

- ERR_P1_PJC_E_LT_1
- ERR_P1_W_LT_1
- ERR_P1_S_LT_1
- ERR_P1_WITHOUT_P1C
- ERR_P1_D1C_E_LT_0PT5
- ADV_P1_WITHOUT_P0



9) MMPOLY1_CUT

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

Incompatible Layers:

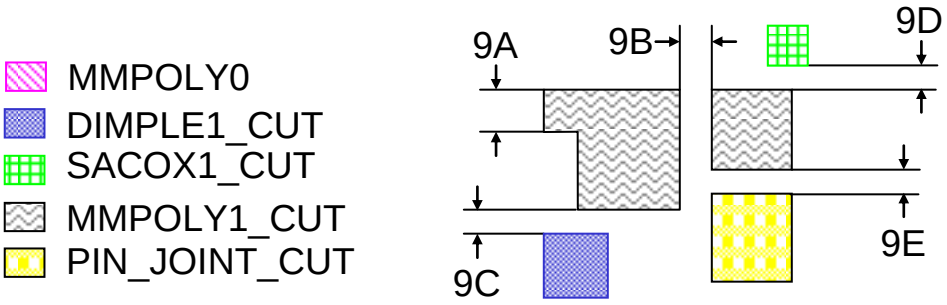
C) DIMPLE1_CUT space = 0.5
D) SACOX1_CUT space = 0.5
E) PIN_JOINT_CUT space = 1.0

Recommended Layers:

Notes:

Errors:

- ERR_P1C_X2_E_LT_0PT5



10) SACOX2

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

Incompatible Layers:

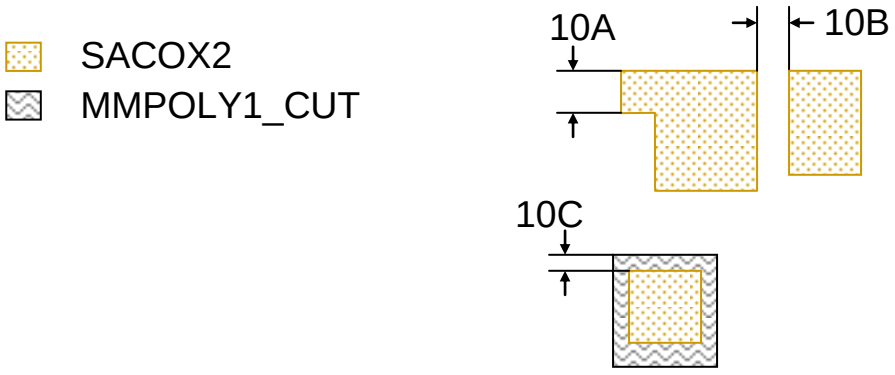
Recommended Layers:

Notes:

C) If SACOX2 is enclosed by MMPOLY1_CUT, MMPOLY1_CUT must enclose SACOX2 by at least 0.5µm.

Errors:

- ERR_X2_W_LT_1
- ERR_X2_S_LT_1



11) SACOX2_CUT

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

C) SACOX2

Incompatible Layers:

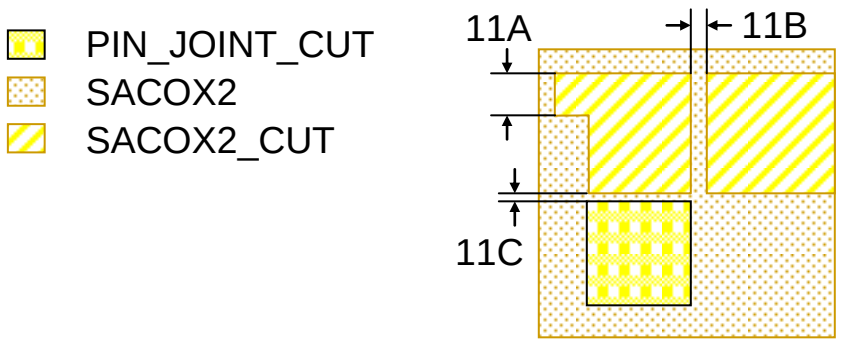
- PIN_JOINT_CUT space = 0.5

Recommended Layers:

Notes:

Errors:

- ERR_X2C_WITHOUT_X2



12) MMPOLY2

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

Incompatible Layers:

Recommended Layers:

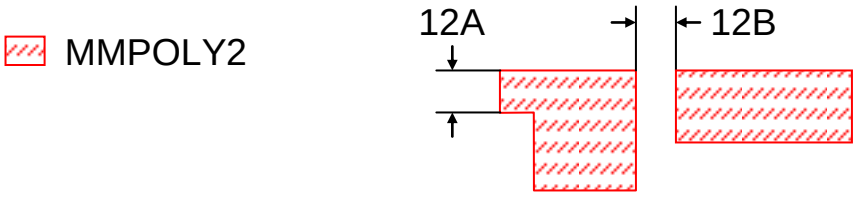
- MMPOLY1 (default) for mechanical rigidity

Notes:

- SACOX3_CUT may not be deep enough to anchor to MMPOLY2 in areas where it overlaps NITRIDE_CUT.

Errors:

- ERR_P2_W_LT_1
- ERR_P2_S_LT_1
- ERR_P2_PJC_E_LT_1
- ADV_P2_X1C_E_LT_0PT5
- ADV_P2_X2_OLAP_LT_0PT5



13) MMPOLY2_CUT

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

C) MMPOLY2

Incompatible Layers:

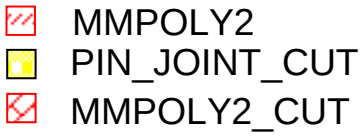
- PIN_JOINT_CUT space = 1.0

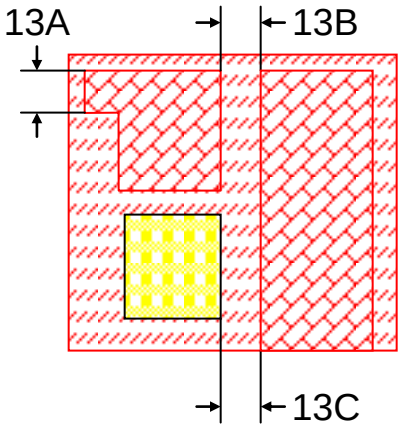
Recommended Layers:

Notes:

Error:

- ERR_P2C_WITHOUT_P2
- ADV_P2_S_GT_38





14) DIMPLE3_CUT

A) MIN WIDTH 1.5
B) MIN SPACE 1.0

Required Layers:

C) MMPOLY3 enclosure of DIMPLE3_CUT = 0.5

Incompatible Layers:

D) SACOX3_CUT space = 1.0
E) MMPOLY3_CUT space = 0.5

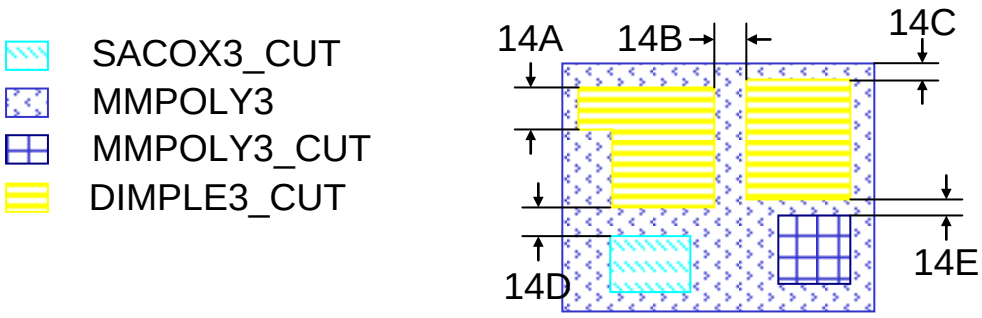
Recommended Layers:

- MMPOLY2 under full DIMPLE3_CUT area

Notes:

Errors:

- ERR_D3C_W_LT_1
- ERR_D3C_S_LT_1
- ERR_D3C_X3C_S_LT_1
- ADV_D3C_WITHOUT_P2



15) SACOX3_CUT

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

C) MMPOLY2 (full height)
Minimum coincident area* = 3.14μm^2
D) MMPOLY3 enclosure of SACOX3_CUT = 0.5

Incompatible Layers:

E) DIMPLE3_CUT space = 1.0
F) MMPOLY3_CUT space = 0.5

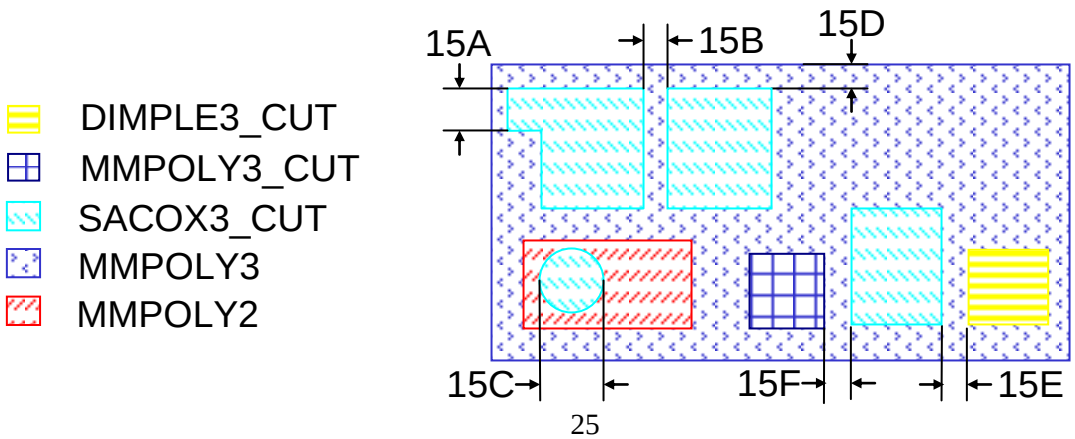
Recommended Layers:

Notes:

- Depending on the design, considerable topography can be generated with underlying layers. This rule only considers the portion of MMPOLY2 that is unaffected in elevation by the removal of any of the underlying layers other than SACOX2 and MMPOLY0, although either or both can be included if desired. The result is then compared to SACOX3_CUT to ensure that a valid anchor region of at least 2μm diameter exists. If this is not the case, the rule is flagged as "invalid SACOX3 anchor".
- *Coincident area is based on 2μm diameter circle.
- For example, SACOX3_CUT may not be deep enough to anchor to MMPOLY2 in areas where it overlaps NITRIDE_CUT.

Errors:

- ERR_X3C_W_LT_1
- ERR_X3C_S_LT_1
- ERR_INVALID_SACOX3_ANCHR
- ERR_X3C_WITHOUT_P2P1



16) MMPOLY3

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

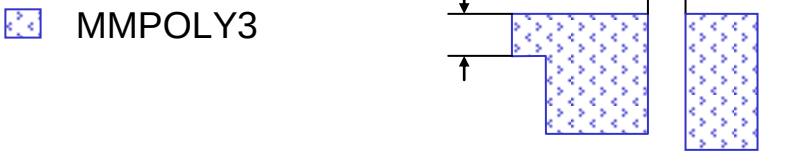
Incompatible Layers:

Recommended Layers:

Notes:

Errors:

- ERR_P3_W_LT_1
- ERR_P3_S_LT_1
- ERR_P3_D3C_E_LT_0PT5
- ERR_P3_X3C_E_LT_0PT5



17) MMPOLY3_CUT

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

- MMPOLY3

Incompatible Layers:

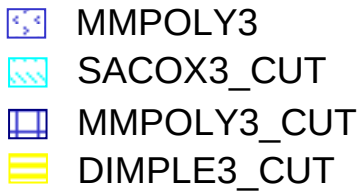
C) DIMPLE3_CUT space = 0.5
D) SACOX3_CUT space = 0.5

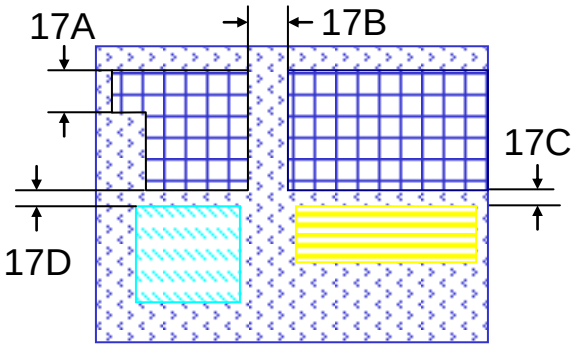
Recommended Layers:

Notes:

Errors:

- ERR_P3C_WITHOUT_P3
- ADV_P3C_SPC_GT_38





18) DIMPLE4_CUT

A) MIN WIDTH 1.5
B) MIN SPACE 1.0

Required Layers:

C) MMPOLY4 enclosure of DIMPLE4_CUT = 0.5

Incompatible Layers:

D) SACOX4_CUT space = 1.0
E) MMPOLY4_CUT space = 0.5

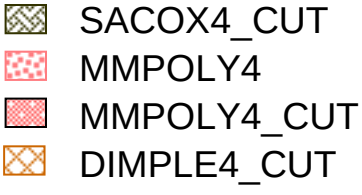
Recommended Layers:

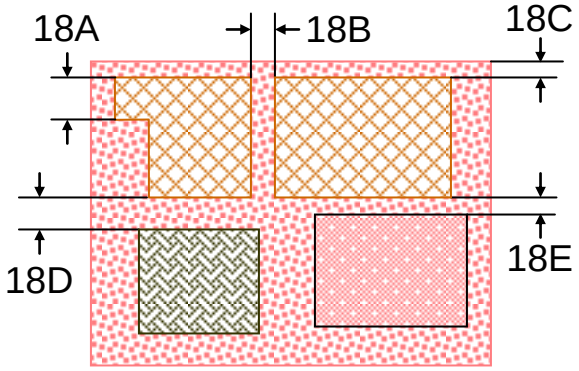
- MMPOLY3 under full DIMPLE4_CUT area

Notes:

Errors:

- ERR_D4C_W_LT_1
- ERR_D4C_S_LT_1
- ERR_D4C_X4C_S_LT_1
- ERR_D4C_P4C_S_LT_0PT5
- ADV_D4C_WITHOUT_P3





19) SACOX4_CUT

A) A) MIN WIDTH 1.0
B) B) MIN SPACE 1.0

Required Layers:

C) MMPOLY3 (full height)

- minimum coincident area* = 3.14 μm^2

D) MMPOLY4 enclosure of SACOX4_CUT = 0.5

Incompatible Layers:

E) DIMPLE4_CUT space = 1.0
F) MMPOLY4_CUT space = 0.5

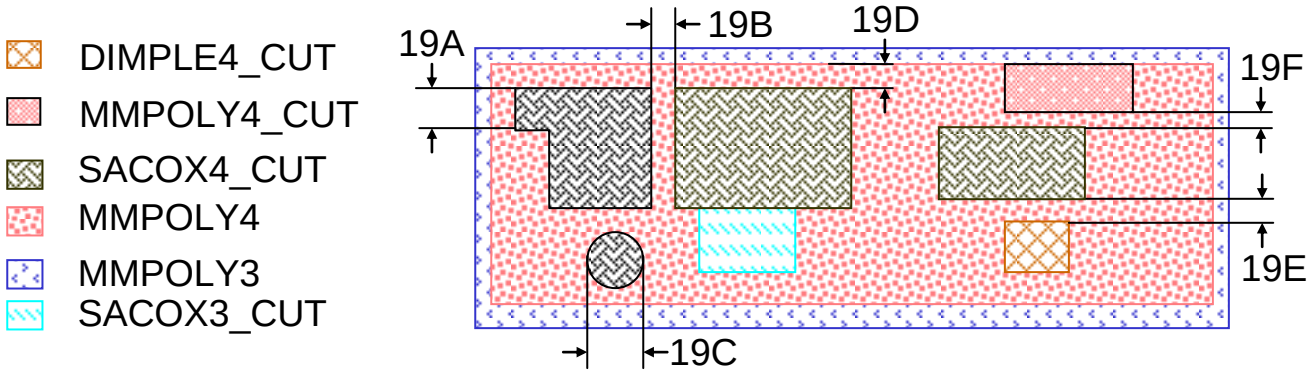
Recommended Layers:

Notes:

- This rule only considers the portion of MMPOLY3 that is unaffected in elevation by the removal of any of the underlying layers. The result is then compared to SACOX3_CUT to ensure that a valid anchor region of at least 2-µm diameter exists. If this is not the case, the rule is flagged as "invalid SACOX4 anchor".
- *Coincident area is based on 2-µm diameter circle.

Errors:

- ERR_X4C_W_LT_1
- ERR_X4C_S_LT_1
- ERR_INVALID_SACOX4_ANCHR
- ERR_X4C_WITHOUT_P3



20) MMPOLY4

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

Incompatible Layers:

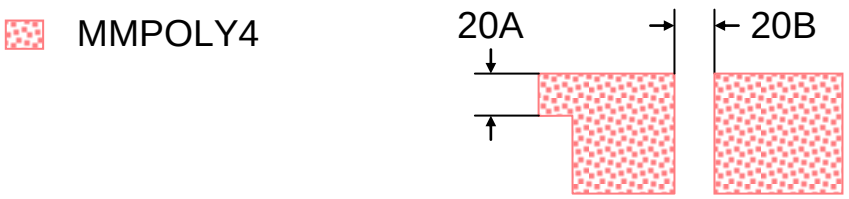
Recommended Layers:

- SACOX4_CUT

Notes:

Errors:

- ERR_P4_W_LT_1
- ERR_P4_S_LT_1
- ERR_P4_D4C_E_LT_0PT5
- ERR_P4_X4C_E_LT_0PT5
- ADV_P4_NOT_TOUCHING_X4C



21) MMPOLY4_CUT

A) MIN WIDTH 1.0
B) MIN SPACE 1.0

Required Layers:

- MMPOLY4

Incompatible Layers:

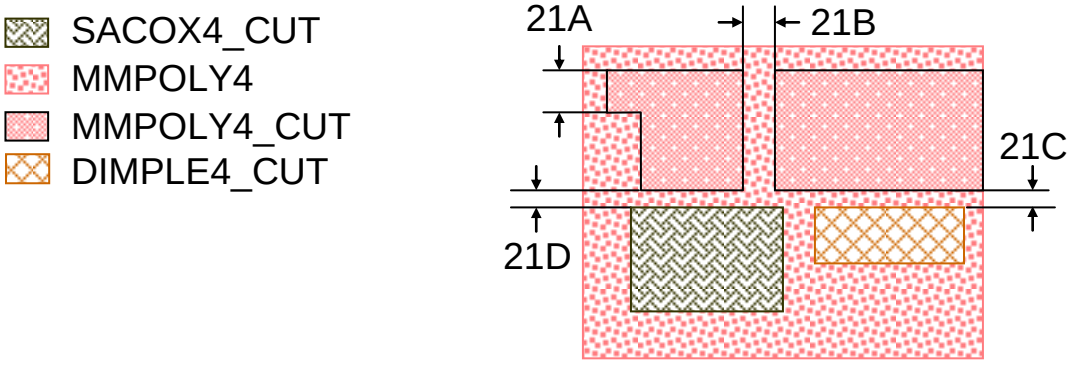
C) DIMPLE4_CUT space = 0.5
D) SACOX4_CUT space = 0.5

Recommended Layers:

Notes:

Errors:

- ERR_P4C_WITHOUT_P4



22) PTNMETAL*

A) MIN WIDTH 6.0
B) MIN SPACE 1.0

Required Layers:

C) MMPOLY4 enclosure of PTNMETAL = 2.0µm
D) PTNMETAL enclosure of SACOX4_CUT = 2.0µm
E) PTNMETAL enclosure of DIMPLE4_CUT = 2.0µm
F) PTNMETAL MMPOLY4_CUT space = 2.0µm

Incompatible Layers:

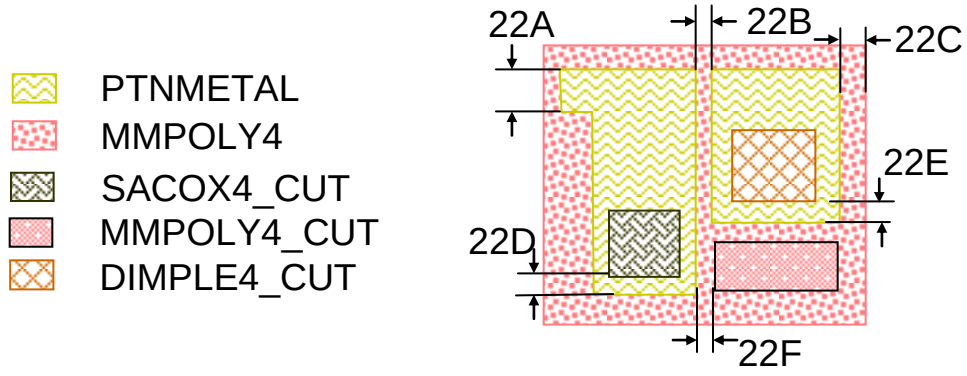
Recommended Layers:

Notes:

- *PTNMETAL is currently available for use on bondpads only. If you have a design which requires a metal deposition on anything other than bondpads, please contact the Sandia National Laboratories process engineer to discuss your design.

Errors:

- ERR_PM_W_LT_6
- ERR_PM_S_LT_1
- ERR_PM_P4_E_LT_2
- ERR_PM_ X4C_E_LT_2
- ERR_PM_ D4C_E_LT_2



23) PTNMETAL_CUT*

A) MIN WIDTH 2.0
B) MIN SPACE 4.0

Required Layers:

C) PTNMETAL enclosure of PTNMETAL_CUT = 4.0µm

Incompatible Layers:

D) SACOX4_CUT space=2.0µm
E) DIMPLE4_CUT space= 2.0µm

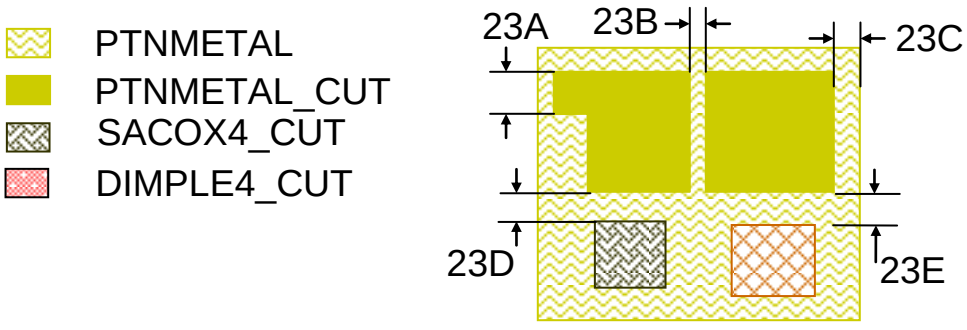
Recommended Layers:

Notes:

- *If you need to use PTNMETAL_CUT in your design please contact the Sandia National Laboratories process engineer to discuss your design needs.

Errors:

- ERR_PMC_WITHOUT_PM



Summary of SUMMiT™ Design Rules

1. Minimum width and space for most layers = 1µm. The exceptions are listed below.
2. DIMPLE3_CUT and DIMPLE4_CUT: width = 1.5 µm, space = 1 µm.
3. PIN_JOINT_CUT: width = 3 µm, space = 1 µm, space for separation of PIN_JOINT_CUTs is at least 4, preferably 7 µm.
4. Minimum overlap tolerance = 0.5 µm for polysilicon and underlying cuts, MMPOLY0 + NITRIDE_CUT, MMPOLY1+DIMPLE1_CUT, MMPOLY1+SACOX1_CUT, MMPOLY3 + SACOX3_CUT, MMPOLY3 + DIMPLE3_CUT, MMPOLY4+SACOX4_CUT, MMPOLY4+DIMPLE4_CUT.

Other Design Rules and Recommendations

1. All layers must either be anchored, attached to substrate, or otherwise held down (no floating parts)
2. For many structures, the nominal dimple spacing should be every 75µm or less. The optimal spacing is very dependent on the design of the structure and could be greater or less than 75µm."
3. Etch release holes should be spaced 38 µm apart or closer.
4. Typical size of etch release holes is 2x2 µm.
5. MMPOLY1 and MMPOLY2 will be sandwiched and etched with the poly2 mask unless there is a SACOX2 layer surrounding the poly, i.e. a SACOX2_CUT is automatic unless specified.
6. MMPOLY1 is defined everywhere unless there is a MMPOLY1_CUT. The only way to actually draw in MMPOLY1 is to have MMPOLY1_CUT and SACOX2 surrounding it.
7. It is recommended that POLY0 be underneath all geometric features.
8. Typical size of etch release holes is 2x2 µm.
9. The following layers are required with PIN_JOINT_CUT: MMPOLY1 (1 µm enclosure), SACOX2 (0.5 µm enclosure), MMPOLY2 (2µm enclosure). PINJOINT_CUT is incompatible with DIMPLE1_CUT, SACOX1_CUT, MMPOLY1_CUT, SACOX2_CUT, and MMPOLY2_CUT. All of the previous layers have a required space of 1µm except for SACOX2_CUT, which has a required space of 0.5µm.
10. Minimum area of MMPOLY1 island defined by PIN_JOINT_CUT = 3.14µm^2.
11. SACOX cuts are breakable with probes if area is less than 50µm2.
12. Although, MMPOLYX and MMPOLYX_CUT are separate layers in AutoCAD, there is only one layer of geometry produced. Except for MMPOLY1, the easiest thing is remember that cut layers are not defined where the main layer (MMPOLYX) does not exist. The purpose of the cut layer is to make it easy to draw holes (for example etch release holes) in the master layer.

Although there are exceptions, all sacox and dimple cuts should have the previously deposited polysilicon layer under them. For example, SACOX3_CUT must have MMPOLY2 underneath it. Also, the depth of dimples and sacox cuts are set assuming that there is no underlying topography. For example, a SACOX3_CUT may not contact the MMPOLY12 if the SACOX3_CUT is over a NITRIDE_CUT. A nitride cut creates a depression in the MMPOLY12. Similarly, a SACOX4 cut above a DIMPLE3_CUT may not contact the underlying MMPOLY3. Another example is a DIMPLE4_CUT that is not over MMPOLY3. Because the dimple etch does not have an etch stop, the DIMPLE4 may extend below the top surface of MMPOLY3 and cause mechanical interference. The safest course is not to have more than one cut coincident with another. The conservative size of these sacox cuts is at least 2µm x 2µm.

Designers should attempt to put all their designs on a 0.05µm grid. When the masks for photolithography are created, the edges of features are snapped to this grid (including arcs and gear teeth). In addition, designers should realize that independent of the processing it is not possible to create features smaller than this on a mask plate in the standard SUMMiT™ process.